criticalblue

Cascade Application Coprocessor

System Power Reduction

The Power Reduction Challenge

A leading consumer products manufacturer was faced with the challenge of implementing an audio codec for deployment in a portable consumer device.

The codec had to operate at 40 frames per second within the usual tight power consumption constraints of portable products.

The codec software itself was open source software. The manufacturer had used it successfully on a previous project, but had no knowledge of its inner workings. Use of the code "as is" with no changes whatsoever was therefore essential – any and all optimizations and trade-offs had to be made purely in hardware.

Moreover, the manufacturer's codec software knowledge gap precluded its conversion for implementation in a fixed function block.

Initially, the manufacturer attempted to re-use the previous design that utilized the ARM926EJ as the central processing unit (CPU). In this design, the algorithm had been required to execute at 25% of real time. However, in order to achieve the new target of 40 frames per second, the processor would have to operate at 504 MHz, which was not feasible. In any case, the power consumption – 226mW in a 130nm process technology – would have been unacceptable.

Application Coprocessor

The manufacturer selected CriticalBlue's Cascade Application Coprocessor synthesis solution to achieve the requisite performance within the power consumption constraints.

A Cascade-synthesized application coprocessor offers the programmability of a processor with the parallel processing performance of a fixed function hardware block. Cascade can rapidly synthesize multiple coprocessors to perform a wide range of power/performance trade-offs. Moreover, the coprocessor is synthesized using compiled binary executable software code developed for single CPU operation, thus fulfilling the manufacturer's "as is" software re-use requirement.

The manufacturer synthesized an application coprocessor for the audio codec. The ARM926 EJ/Cascade coprocessor configuration delivered the requisite processing performance with a power consumption 47% lower than that of the stand-alone 926EJ (see table 1). However, the 65% increase in processor sub-system's silicon area was very undesirable in such a high volume product.

It was determined that – in this configuration – the 926EJ's contribution to codec processing was minimal. The manufacturer therefore replaced it with an ARM7EJ processor. The ARM7EJ/Cascade coprocessor configuration consumed 60% less power than the stand-alone 926EJ, and used 12% less silicon area, in part because the ARM7EJ contains no cache memory.

The Cascade coprocessor thus enabled the manufacturer not only to achieve the requisite performance within the power constraints, but also to deploy a lower cost, smaller footprint CPU.

All in One Day

Synthesis of the audio application processor required one engineer day of effort.

	System Power Reduction		
	ARM926EJ	**ARM926EJ + Coprocessor**	**ARM7EJ + Coprocessor**
Power consumption (mW)	226	119	91
Power Consumption Change vs. 926	-	(47%)	(60%)
Area (mm^2)	3.2	5.3	2.8
Area Change vs. 926	-	65%	(12%)
CPU Clock Rate (MHz)	504	90	90
Coprocessor Clock Rate (MHz)	-	152	152

Table 1: System Power Reduction